

**CLAIM AMENDMENTS**

Please amend the claims as described below. In accordance with 37 CFR §1.121, a complete listing of all claims in the application is provided below. Notably, the status of each claim is indicated in the parenthetical expression adjacent to the corresponding claim number.

1           1. **(Currently Amended)** A semiconductor memory array, comprising:  
2           a plurality of semiconductor dynamic random access memory cells arranged in a  
3           matrix of rows and columns, each semiconductor dynamic random access memory cell  
4           includes at least one transistor having:  
5                 a source region;  
6                 a drain region;  
7                 a body region disposed between and adjacent to the source region and the  
8           drain region, wherein the body region is electrically floating; and  
9                 a gate spaced apart from, and capacitively coupled to, the body region;  
10          wherein each memory cell transistor includes (1) a first data state which  
11          corresponds to representative of a first charge in the body region of the transistor of the  
12          memory cell, and (2) a second data state which corresponds to representative of a second  
13          charge in the body region of the transistor of the memory cell; and  
14          wherein the source region of the transistor of each memory cell corresponding to a  
15          first each row of semiconductor dynamic random access memory cells is connected to the  
16          same includes an associated source line which is connected to only the semiconductor  
17          dynamic random access memory cells of the associated row and wherein the gate of the

18 transistor of each memory cell corresponding to the first row of semiconductor dynamic  
19 random access memory cells is connected to the same word line.

1       2. (Currently Amended) The semiconductor memory array of claim 1 wherein the  
2 drain region of the transistor of each memory cell of each the first row of semiconductor  
3 dynamic random access memory cells ~~includes~~ is connected to a separate different bit line  
4 ~~which is connected to the drain region of the associated transistor.~~

1       3. (Currently Amended) The semiconductor memory array of claim 2 wherein  
2 each memory cell of a the first row is programmed to a the first data state by applying a  
3 control signal, having a first amplitude, to the gate of the transistor of each memory cell of  
4 the first row and a control signal, having a second amplitude, to the drain region of the  
5 transistor of each memory cell of the first row.

1       4. (Currently Amended) The semiconductor memory array of claim 3 wherein a  
2 predetermined memory cell of the first row is programmed to a second data state by  
3 applying (1) a control signal, having a third amplitude, to the gate of the transistor of the  
4 predetermined memory cell, (2) a control signal, having an fourth amplitude, to the drain  
5 region of the transistor of predetermined memory cell, and (3) a control signal, having a  
6 fifth amplitude, to the source region of the transistor of predetermined memory cell of the  
7 first row.

1           5. (Currently Amended) The semiconductor memory array of claim 4 wherein an  
2 unselected memory cell of the first row is maintained in the first data state, while the  
3 predetermined memory cell is programmed to a the second data state, by applying a  
4 control signal, having a the third amplitude, to the gate of the transistor of the  
5 predetermined unselected memory cell and a control signal, having an sixth amplitude, to  
6 the drain region of the transistor of ~~predetermined~~ the unselected memory cell.

1           6. (Currently Amended) The semiconductor memory array of claim 5 wherein all  
2 of the predetermined memory cells ~~of the first row are~~ is read by applying a control signal,  
3 having a seventh amplitude, to the gate of the transistor of the predetermined memory cell  
4 and a control signal, having an eight amplitude, to the drain region of the transistor of  
5 predetermined memory cell.

1           7. (Currently Amended) The semiconductor memory array of claim 6 wherein all  
2 of the memory cells of a second row are maintained in an inhibit state while the  
3 predetermined memory cells of the first row is are read.

1           8. (Currently Amended) The semiconductor memory array of claim 6 wherein all  
2 of the memory cells of a second row are maintained in an inhibit state while the  
3 predetermined memory cells of the first row is are read by applying a control signal<sub>1</sub> having  
4 a ninth amplitude<sub>1</sub> to the gate of each ~~the~~ transistors of the memory cells of the second  
5 row.

1           9. (Currently Amended) The semiconductor memory array of claim 1 wherein the  
2 transistor of each memory cell of a the first row of semiconductor dynamic random access  
3 memory cells shares a drain region with a transistor of an adjacent memory cell in of a  
4 second row of semiconductor dynamic random access memory cells, wherein the first and  
5 second rows of memory cells are adjacent rows.

1           10. (Currently Amended) The semiconductor memory array of claim ~~9~~1 wherein  
2 ~~each~~ the gate of the transistor of each memory cell of a the first second row of  
3 semiconductor dynamic random access memory cells is connected to a first second gate  
4 word line.

1           11. (Currently Amended) The semiconductor memory array of claim 10 wherein  
2 the source region of the transistor of each memory cell of the second row of semiconductor  
3 dynamic random access memory cells is connected to a common source line only the gate  
4 of each memory cell of the first row of semiconductor dynamic random access memory  
5 cells is connected to the first gate line.

1           12. (Currently Amended) A semiconductor memory array, comprising:  
2 a plurality of semiconductor dynamic random access memory cells arranged in a  
3 matrix of rows and columns, each semiconductor dynamic random access memory cell  
4 includes at least one transistor having:  
5 a source region;

6 a drain region;  
7 a body region disposed between ~~and adjacent to~~ the source region and the  
8 drain region, wherein the body region is electrically floating; and  
9 a gate spaced apart from, and capacitively coupled to, the body region;  
10 wherein each transistor includes a first state representative of a first charge in the  
11 body region, and a second data state representative of a second charge in the body region;  
12 wherein the source region of the transistor of each memory cell corresponding to  
13 each a first row of semiconductor dynamic random access memory cells is connected to a  
14 first includes (1) an associated source line which is connected to only the semiconductor  
15 dynamic random access memory cells in the associated row and (2) a different wherein the  
16 gate line for of the transistor of each memory cell corresponding to the first row of each  
17 semiconductor dynamic random access memory cells in the associated row is connected  
18 to a first word line;  
19 wherein the source region of the transistor of each memory cell corresponding to a  
20 second row of semiconductor dynamic random access memory cells is connected to a  
21 second source line and wherein the gate of the transistor of each memory cell  
22 corresponding to the second row of semiconductor dynamic random access memory cells  
23 is connected to a second word line; and  
24 wherein the first and second rows of semiconductor dynamic random access  
25 memory cells are adjacent rows.

1 13. (Currently Amended) The semiconductor memory array of claim 12 wherein  
2 the drain region of the transistor of each memory cell of each the first row of semiconductor

3 dynamic random access memory cells ~~includes~~ is connected to a separate different bit line  
4 ~~which is connected to the drain region of the associated transistor.~~

1 14. (Currently Amended) The semiconductor memory array of claim 13 wherein  
2 each memory cell of a the first row is programmed to a first data state by applying a control  
3 signal, having a first amplitude, to the gate of the transistor of each memory cell of the first  
4 row and a control signal, having a second amplitude, to the drain region of the transistor of  
5 each memory cell of the first row.

1 15. (Currently Amended) The semiconductor memory array of claim 14 wherein a  
2 predetermined memory cell of the first row is programmed to a second data state by  
3 applying a control signal, having a third amplitude, to the gate of the transistor of the  
4 predetermined memory cell, a control signal, having an fourth amplitude, to the drain region  
5 of the transistor of the predetermined memory cell, and a control signal, having a fifth  
6 amplitude, to the source region of the transistor of the predetermined memory cell of the  
7 first row.

1 16. (Currently Amended) The semiconductor memory array of claim 15 wherein  
2 an unselected memory cell of the first row is maintained in the first data state, while the  
3 predetermined memory cell is programmed to a the second data state, by applying a  
4 control signal, having a third amplitude, to the gate of the transistor of the unselected  
5 ~~predetermined~~ memory cell and a control signal, having an sixth amplitude, to the drain  
6 region of the transistor of the unselected ~~predetermined~~ memory cell.

1           17. (Currently Amended) The semiconductor memory array of claim 16 wherein  
2 all of the memory cells of the first row are read by applying a control signal, having a  
3 seventh amplitude, to the gate of the transistor of ~~the predetermined~~ each memory cell of  
4 the first row, and a control signal, having an eight amplitude, to the drain region of the  
5 transistor of each ~~predetermined~~ memory cell of the first row.

1           18. (Currently Amended) The semiconductor memory array of claim 17 wherein  
2 all of the memory cells of ~~a~~ the second row are maintained in an inhibit state while the  
3 memory cells of the first row are read.

1           19. (Currently Amended) The semiconductor memory array of claim 17 wherein  
2 all of the memory cells of ~~a~~ the second row are maintained in an inhibit state while the  
3 memory cells of the first row are read by applying a control signal having a ninth amplitude  
4 to the gate of the transistors of each ~~the~~ memory cells of the second row.

1           20. (Currently Amended) The semiconductor memory array of claim 12 wherein  
2 the transistor of each memory cell of ~~a~~ the first row of semiconductor dynamic random  
3 access memory cells shares a drain region with the transistor of an adjacent memory cell in  
4 ~~a~~ the second row of semiconductor dynamic random access memory cells, ~~wherein the first~~  
5 ~~and second rows of memory cells are adjacent rows~~.